REMARKS

In the Office Action, the Examiner required a new title, rejected claims 1, 2, 5 – 11 and 14 as obvious over Sexton et al. in view of Kato et al., rejected claim 3 as obvious over Sexton et al, in view of Kato et al. and further in view of Solari, rejected claim 4 as obvious in view of Sexton and Kato in view of Bowes et al., indicated that claims 12 and 13 are directed to allowable subject matter, and identified further art of record but not relied upon.

Title Objection

The title is amended as set forth above. Applicants submit that the new title describes the invention being claimed.

35 USC 103(a)

The Sexton et al. reference does not show that a bus controller of a transmitter programs the DMA to read out the stored data from memory and send the data to the receiver in response to a request message from the receiver.

The Examiner notes that Sexton et al. disclose a plurality of modules connected to a parallel bus wherein each module includes a processor, a memory device and a DMA controller. Data can be transmitted via a parallel databus without the use of the processor. This is a common and known purpose of DMAs. However, before the transmission of data via DMAs is started, the corresponding DMA has to be programmed. Therefore, the address of the data which are to be transmitted and the amount of data bytes which are to be transmitted have to be entered into the DMA. This entering of the data into a DMA is in the present patent application called "programming of the DMA". All ordinary devices using a DMA for data transmission are using a CPU for programming the DMA.

Further, the Examiner notes that Kate at al. disclose a system wherein the first CPU la is programming the first DMA 2a to transmit data to the unit lob (Figure 2). This is the ordinary way that DMAs are programmed, namely by the CPU which is provided on the assembly of the corresponding DMA.

The present invention comprises a transmitter assembly end a receiver assembly. The receiver assembly creates a data request message (see last paragraph on page 6 of the present application). The data request message contains the address of the data in the memory and the amount of data bytes that are to be transmitted and a so called duty cycle for the transmission of the requested messages. This data request message is sent to the transmitter assembly and the address of the data, the amount of the data bytes and the duty cycle are programmed by the bus controller and not the CPU of the transmitter assembly into the DMA of the transmitter assembly, whereby the data transmission is started without making use of the processor of the transmitter assembly.

This is contrary to the disclosure of Kato at al., where the CPU 1b of the assembly 10a programs the DMA 2a of this assembly. The Kato reference does not disclose that a CPU of a certain assembly programs the DMA of another assembly.

By the present invention, the data for programming the DMA are created by the processor of the receiver assembly, transmitted to the transmitter assembly and programmed without use of the processor into the DMA of the transmitter assembly. Thus, it can be said that the CPU of the receiver assembly programs a DMA at the transmitter assembly. This is the gist of the invention which is neither disclosed in the cited prior art nor does the cited art provide any suggestions for such a solution. As such, the claimed invention is non-obvious over the combination of Sexton and Kato.

The Solari reference does not show or suggest the features noted above and so the claimed invention is non-obvious over the combination of Sexton, Kato and Solari.

The Bowes reference also does not show or suggest the features noted above and so the claimed invention is non-obvious over the combination of Sexton, Kato and Bowes.

Additional Art

The additional art cited by the Examiner but not relied upon is noted by the Applicants.

Conclusion

Applicants respectfully favorable reconsideration and allowance of the present application in view of the foregoing remarks.

Respectfully submitted,

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CH1\4143735.1